a binding layer formed on said dielectric layer and on said exposed portion of a surface of said first layer;

a second layer of conductive material formed on said binding layer;

a layer of variable resistance material formed over said second layer of conductive material, said variable resistance material being able to change resistance under the influence of an applied voltage; and

a third layer of conductive material formed over said layer of variable resistance material.

78. The memory cell of claim 77, wherein said second layer of conductive material is a metal layer and said binding layer comprises an oxide layer and metal from said second layer diffused into said oxide layer.

Cl Cont.

79. A memory system, comprising:

an array of memory elements, each memory element including:

a first layer of conductive material;

a dielectric layer formed on a surface of said first layer;

an opening formed in the dielectric layer to expose a portion of a surface of said first layer;

a binding layer formed on said dielectric layer and on said exposed portion of a surface of said first layer;

a second layer of conductive material formed on said binding layer;

a layer of variable resistance material formed over said second layer of conductive material, said variable resistance material being able to change resistance under the influence of an applied voltage; and

a third layer of conductive material formed over said variable resistance material.

80. The memory system of claim 79, wherein said second layer of conductive material is a metal layer and said binding layer comprises an oxide layer and metal from said second layer diffused into said oxide layer.

81. An electronic system, comprising:

a processor; and

a memory system coupled to the processor, said memory system comprising at least one memory element including:

a' cont.

a first layer of conductive material;

a dielectric layer formed on a surface of said first layer;

an opening formed in said dielectric layer to expose a portion of a surface of said first layer;

a binding layer formed on the dielectric layer and on the exposed portion of a surface of said first layer;

a second layer of conductive material formed on said binding layer;

a layer of variable resistance material formed over said second layer of conductive material, said resistance variable resistance being able to change resistance under the influence of an applied voltage; and

a third layer of conductive material formed over said variable resistance material.

82. The electronic system of claim 81, wherein said second layer of conductive material is a metal layer and said binding layer comprises an oxide layer and metal from said second layer diffused into said oxide layer.

83. A method of making a memory cell, comprising:

forming a first layer of conductive material;

forming a dielectric layer on a surface of the first layer;

forming an opening in said dielectric layer to expose a portion of a surface of said first layer;

forming a binding layer on said dielectric layer and on said exposed portion of a surface of said first layer;

forming a second layer of conductive material on said binding layer;

forming a layer of variable resistance material over said second layer of conductive material, said variable resistance material being able to change resistance under the influence of an applied voltage; and

forming a third layer of conductive material over said layer of variable resistance material.

84. The method of making a memory cell of claim 83, wherein said second layer of conductive material is a metal layer and said binding layer comprises an oxide layer and metal from said second layer diffused into said oxide layer.

85. A method of making a memory system, comprising:

forming an array of memory elements; and

forming a memory cell associated with each memory element, wherein

forming each memory cell includes:

forming a first layer of conductive material;

forming a dielectric layer on a surface of the first layer; forming an opening in the dielectric layer to expose a portion of the surface of the first layer;

forming a binding layer on the dielectric layer and on the exposed portion of a surface of said first layer;

forming a second layer of conductive material on the binding layer;

forming a layer of variable resistance material over said second layer of conductive material, said variable resistance material being able to change resistance under the influence of an applied voltage; and

forming a third layer of conductive material over said layer of variable resistance material.

86. The method of making a memory system of claim 85, wherein said second layer of conductive material is a metal layer and said binding layer comprises an oxide layer and metal from said second layer diffused into said oxide layer.

87. A method of making an electronic system, comprising:

forming a processor; and

forming a memory system coupled to the processor, wherein forming the memory system includes:

forming an array of memory elements; and

forming a memory cell associated with each memory element, wherein forming each memory cell includes:

forming a first layer of conductive material;

forming a dielectric layer on a surface of the first layer;

forming an opening in the dielectric layer to expose a portion of a surface of said first layer;

forming a binding layer on the dielectric layer and on the exposed portion of the surface of the first layer;

a' cont

forming a second layer of conductive material on the binding layer;

forming a layer of variable resistance material over said second layer of conductive material, said variable resistance material being able to change resistance under the influence of an applied voltage; and

forming a third layer of conductive material on said layer of variable resistance material.

88. The method of making an electronic system of claim 87, wherein said second layer of conductive material is a metal layer and said binding layer comprises an oxide layer and metal from said second layer diffused into said oxide layer.

89. A memory cell, comprising:

a first layer of conductive material;

a binding layer formed on a surface of said first layer;

a second layer of conductive material formed on said binding layer;

a layer of variable resistance material formed over said second layer of conductive material, said variable resistance material being able to change resistance under the influence of an applied voltage; and

a third layer of conductive material formed over said layer of variable resistance material.

90. The memory cell of claim 89, wherein said second layer of conductive material is a metal layer and said binding layer comprises an oxide layer and metal from said second layer diffused into said oxide layer.

A' cont.

91. A memory system, comprising:

an array of memory elements, each memory element including:

a first layer of conductive material;

a binding layer formed on a surface of said first layer;

a second layer of conductive material formed on said binding layer;

a layer of variable resistance material formed over said second layer of conductive material, said variable resistance material being able to change resistance under the influence of an applied voltage; and

a third layer of conductive material formed over said variable resistance material.

92. The memory system of claim 91, wherein said second layer of conductive material is a metal layer and said binding layer comprises an oxide layer and metal from said second layer diffused into said oxide layer.

97. A semiconductor die, comprising:

a substrate; and

an integrated circuit supported by the substrate, wherein the integrated circuit includes at least one electrode, the at least one electrode including:

a first layer of conductive material;

a binding layer formed on a surface of said first layer; and

a second layer of conductive material formed on the conductive binding layer.

98. The semiconductor die of claim 97, wherein said second layer of conductive material is a metal layer and said binding layer comprises an oxide layer and metal from said second layer diffused into said oxide layer.

A' cont.

99. A method of making a memory cell, comprising:

forming a first layer of conductive material;

forming a binding layer on a surface of said first layer;

forming a second layer of conductive material on said binding layer;

forming a layer of variable resistance material over said second layer of conductive material, said variable resistance material being able to change resistance under the influence of an applied voltage; and

forming a third layer of conductive material over said layer of variable resistance material.

93. An electronic system, comprising:

a processor; and

a memory system coupled to the processor, said memory system comprising an at least one memory element, each memory element including:

a first layer of conductive material;

a binding layer formed on a surface of said first layer;

a second layer of conductive material formed on said binding layer;

a layer of variable resistance material formed over said second layer of conductive material, said resistance variable resistance being able to change resistance under the influence of an applied voltage; and

a third layer of conductive material formed over said variable resistance material.

94. The electronic system of claim 93, wherein said second layer of conductive material is a metal layer and said binding layer comprises an oxide layer and metal from said second layer diffused into said oxide layer.

95. An electrode structure, comprising:

a first layer of conductive material;

a binding layer formed on a surface of the first layer; and

a second layer of conductive material formed on the conductive binding layer.

96. The electrode structure of claim 95, wherein said second layer of conductive material is a metal layer and said binding layer comprises an oxide layer and metal from said second layer diffused into said oxide layer.

100. The method of making a memory cell of claim 99, wherein said second layer of conductive material is a metal layer and said binding layer comprises an oxide layer and metal from said second layer diffused into said oxide layer.

101. A method of making a memory system, comprising:

forming an array of memory elements; and

forming a memory cell associated with each memory element, wherein

forming each memory cell includes:

forming a first layer of conductive material;

forming a dielectric layer on a surface of the first layer; forming an opening in the dielectric layer to expose a portion of a surface of said first layer;

forming a binding layer on the dielectric layer and on the exposed portion of the surface of the first layer;

forming a second layer of conductive material on the binding layer;

forming a layer of doped chalcogenide material on the second layer of conductive material; and

forming a third layer of conductive material on the layer of doped chalcogenide material.

102. The method of making a memory system of claim 101, wherein said conductive binding layer comprises an oxide layer and metal from said second layer diffused into said oxide layer.

103. A method of making an electronic system, comprising:

forming a processor; and

forming a memory system coupled to the processor, wherein forming the memory system includes:

forming an array of memory elements; and

forming a memory cell associated with each memory element, wherein forming each memory cell includes:

forming a first layer of conductive material;

forming a binding layer on a surface of said first layer;

forming a second layer of conductive material on said binding layer;

forming a layer of variable resistance material over said second layer of conductive material, said variable resistance material being able to change resistance under the influence of an applied voltage; and

forming a third layer of conductive material on said layer of variable resistance material.

104. The method of making an electronic system of claim 103, wherein said second layer of conductive material is a metal layer and said binding layer comprises an oxide layer and metal from said second layer diffused into said oxide layer.

105. A method of making an electrode structure, comprising:

forming a first layer of conductive material;

forming a binding layer on a surface of said first layer; and

forming a second layer of conductive material on the binding layer.

106. The method of making an electrode structure of claim 105, wherein said second layer of conductive material is a metal layer and said binding layer comprises an oxide layer and metal from said second layer diffused into said oxide layer.

107. A method of making a semiconductor die, comprising:

providing a substrate;

forming an integrated circuit supported by the substrate; and

forming an electrode coupled to the integrated circuit, wherein forming the electrode includes:

forming a first layer of conductive material;

forming a binding layer on a surface of said first layer; and

forming a second layer of conductive material on the conductive binding layer.

108. The method of making a semiconductor die of claim 107, wherein said second layer of conductive material is a metal layer and said binding layer comprises an oxide layer and metal from said second layer diffused into said oxide layer.